

# Power and Delay Characterization on Full Adder Performance

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**Abstract**— *The 1-bit full adder circuit is a very important component in the design of application specific integrated circuits. Here, the full adders are designed for the comparison of delay, power consumption, and power-delay product. These include three new full- adder circuits namely the standard adder, the data driven dynamic logic and the split-path data driven dynamic logic. By optimizing the transistor size in each stage the power and delay are minimized. The investigation has been carried out with properly defined simulation that runs on a Cadence VIRTUOSO environment using a 45-nm, 90-nm and 180-nm CMOS technology. The comparisons between these full adders have been done to show the better performance in terms of power consumption, area (number of transistors) and delay. These circuits are suitable for arithmetic circuits and other VLSI applications with very low power consumption and very high speed performance.*

**Index Terms** - Cadence Virtuoso, Data driven dynamic logic, Full adders, Generate, Propagate, Power delay product, Split path data driven dynamic logic.

## 1 Introduction

Adder is one of the most important components of a CPU (central processing unit), Arithmetic logic unit (ALU), floating point unit and address generation like cache or memory access unit use it. In addition, Full- adders are important components in other applications such as digital signal processors (DSP) architectures and microprocessors. Arithmetic functions such as 'addition', 'subtraction', 'multiplication' and 'division' are some examples, which use 'adder' as a main building block. As a result, design of a high-performance full-adder is very useful and important[2].

As we know there are different types of adders. It includes the CMOS standard adder, the mirror adder, the multiplexer-based adder, the transmission gate based adder, the hybrid full adder, the majority full adder etc[3]. Here, the popular adder structures are implemented in the

CMOS 45-nm, 90-nm and 180-nm process technology and analyzed for performance, power, area and delay. The adders selected for the implementation are the standard adder, the data driven dynamic logic and the split-path data driven dynamic logic. Each of the full adders are classified according to the logic function that is realized. Using this approach we have presented an analysis of the possible impact of logic function choice and not just circuit choice on the performance of the final adder[3].

Three different adder functions are realized using the proposed data driven dynamic logic (D3L) and split-precharge data driven dynamic logic (sp-D3L). These implemented full adders can find its application in a ripple carry adder (RCA) and Wallace Tree multiplier to carry out the delay, power and power-delay product on the performance of full adders as well as the systems that employ them[3].

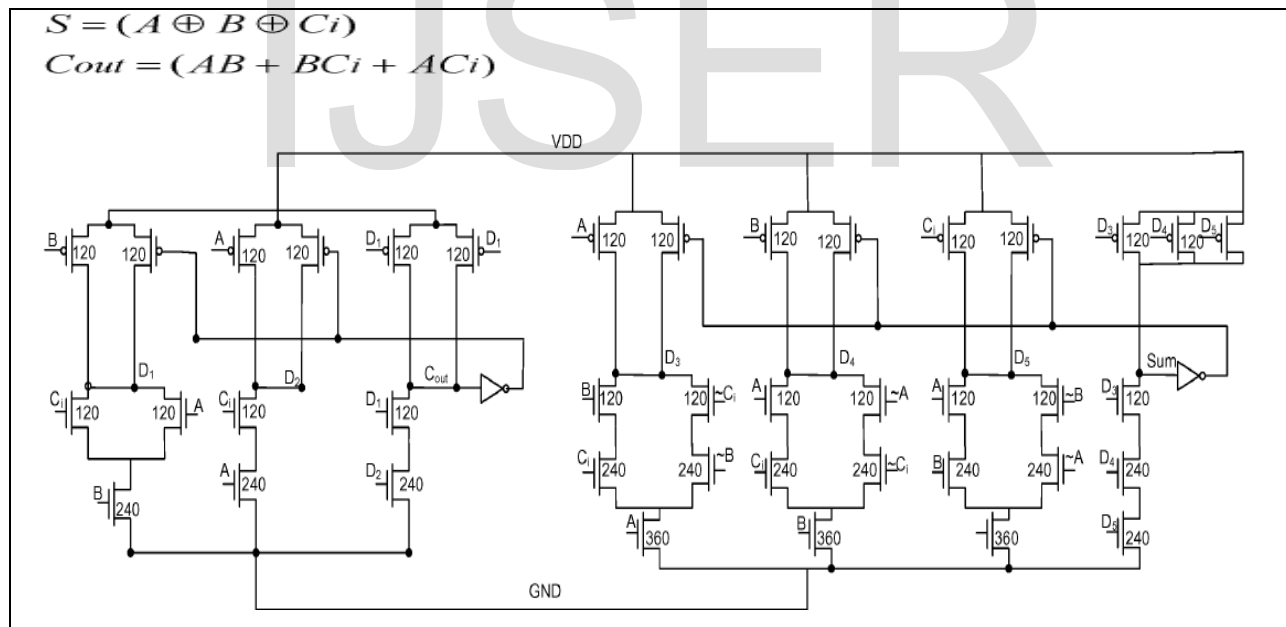
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The performance of a full adder circuit depends on the logic function realized using the particular design style. For instance, a standard CMOS implementation allows circuits to achieve a reasonable power delay product (PDP). Dynamic implementations on the other hand may yield an extremely fast design but end up paying higher costs in the overall power consumption[3]. D3L and sp-D3L are two design styles which allow high performance dynamic circuit design without the additional power consumption in the clock distribution network. Thus these styles form interesting implementation strategies for realizing high performance, power-efficient full adders[3].

## 2 PROPOSED FULL ADDERS

During the design of an adder we have to make two choices in regard to different design abstraction levels. One is responsible for the adder's architecture implemented with the one-bit full adder as a building block. The other defines the specific design style at transistor level to implement the one-bit full adder[1]. The one-bit full adder used is a three-input two-output block. The inputs are the two bits to be summed A and B, and the carry bit  $C_i$ , which derives from the calculations of the previous digits. The outputs are the result of the sum operation and the resulting value of the carry bit  $C_{out}$ .



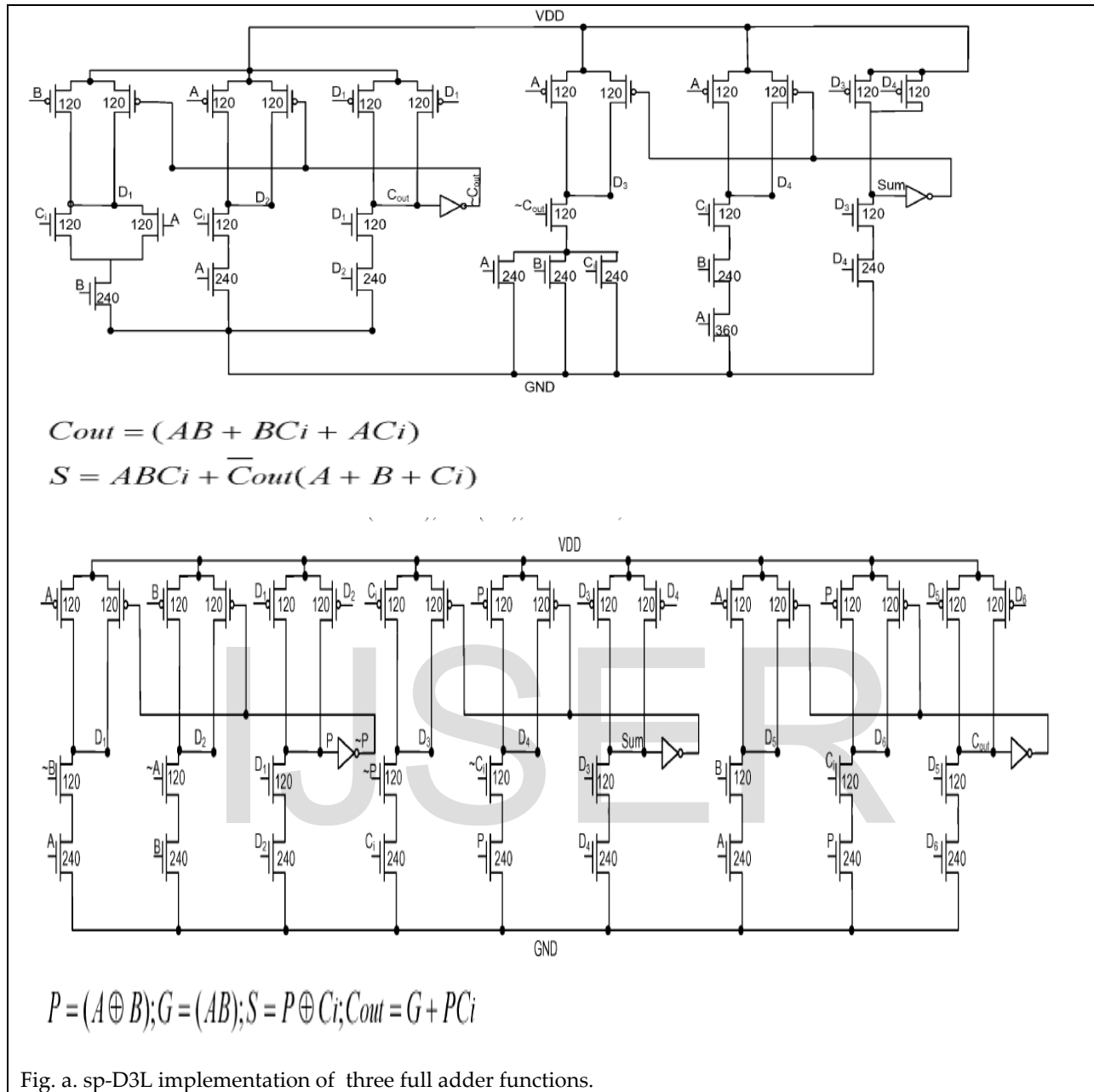


Fig. a. sp-D3L implementation of three full adder functions.

For the simulation of a full adder, there are two important facts. One is the type of design style used for the implementation and the other is the realized logic function. The first figure represents the standard CMOS implementation which allows the circuit to achieve a good power delay product. The number of transistors used for the CMOS standard adder is 40. The circuit is analysed by assigning a 1 bit value for the inputs. Here, if the circuit makes use of more number of transistors then the circuit gives more delay. So,

the sizing of the transistors plays a very important role. Hence, the sizing of the transistors is done in the next two adders, i.e. the Dynamic implementations. The Dynamic implementations are fast but the power consumption is high. The second and third figure is the D3L and sp-D3L are the two design styles for realizing the high performance, power efficient full adders. And in sp-D3L adder, we make use of the GENERATE and PROPAGATE signals for the best performance of the adder circuit.

The sizing of the transistors plays a very important role in the optimization of the circuit performance, power consumption, noise margins, fan-in, fan-out etc. so, the sizing of the transistors gives a best power-delay product by maintaining the drivability of the adders. So, the D3L adders are sized to reduce the delay. The adder circuits are implemented in CMOS 90nm and 180nm technology. The main drawback of these adders is the high power consumption due to large number of transistors and multiple paths to the ground. Here the table represents the comparison of the full adders in terms of delay, power and power delay product.

The power, delay and the P.D.P in the earlier paper is done in IBM 90nm process [3] and the values are tabulated in the below table table 1.

Table 1. The Sum and Carry Delays, Power and the P.D.P for all the three adders in 90nm IBM technology.

Adder Type	Delay		Power		P.D.P(W-s)	
	Sum	Carry	Sum	Carry	Sum	Carry
Standard adder	85ps	75ps	14.16uW	31.71uW	$1203.6 \times 10^{-18}$	$2378.25 \times 10^{-18}$
D3L adder	100ps	82ps	11.484uW	8.982uW	$1148.48 \times 10^{-18}$	$734.54 \times 10^{-18}$
Sp-D3L adder	38ps	42ps	24.29uW	44.586uW	$923.02 \times 10^{-18}$	$1827.61 \times 10^{-18}$

Now, the adders are designed and simulated in Cadence Virtuoso using GPDK tool kit under laboratory conditions and compared and tabulated below in table 2, table3 and table4.

Table 2. The Sum and Carry Delays, Power and the P.D.P for all the three adders in 45nm CMOS technology.

Adder Type	No of transistors	Delay(s)		Power(W)	P.D.P(W-s)	
		Sum	Carry	Average	Sum	Carry
Standard adder	40	81.77ps	50.07ns	152.8mW	12.49p	7.65n
D3L adder	28	150.1ns	50.07ns	135.2mW	20.29n	6.76n
Sp-D3L adder	36	85.07ps	50.07ns	145.8mW	12.40p	7.30n

Table 3. The Sum and Carry Delays, Power and the P.D.P for all the three adders in 90nm CMOS technology.

Adder Type	No of transistors	Delay(s)		Power(W)	P.D.P(W-s)	
		Sum	Carry	Average	Sum	Carry
Standard adder	40	33.82ps	50.02us	293.6mW	9.92p	14.68u
D3L adder	28	75.20ps	50.07ns	261.6mW	19.67p	13.09n
Sp-D3L adder	36	16.74ns	108.4ns	271.6mW	4.54n	29.44n

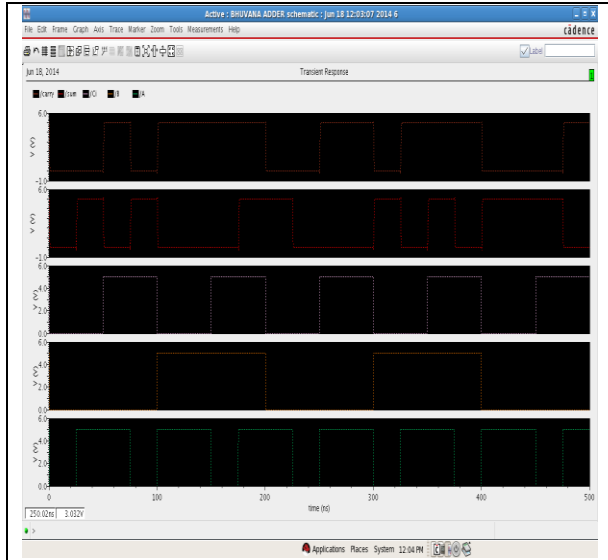
Table 4. The Sum and Carry Delays, Power and the P.D.P for all the three adders in 180nm CMOS technology.

Adder Type	No of transistors	Delay(s)		Power(W)	P.D.P(W-s)	
		Sum	Carry	Average	Sum	Carry
Standard adder	40	286ps	50.26ns	167.9mW	48.01p	8.43n
D3L adder	28	284.6ps	50.64ns	136.8mW	38.93p	6.92n
Sp-D3L adder	36	16.72ns	91.74ns	179.2mW	2.99n	16.43n

### 3 RESULT

When we compare the three different adders, the D3L adder uses less number of transistors than the other two adders. Hence, the delay of the D3L adder is less and the consumption of the power too, is less when compared to the other adders. So, the P.D.P is less for the D3L adder. When compared to 90nm CMOS technology, 180nm has more delay, consumes less power. The adder with more number of transistors has more delay and consumes more power than the adder with the less number of transistors. And the comparison is done in the table.

Below represents the simulation results of the proposed full adders.



The Standard, D3L and sp-D3L adder in 45nm technology has a average sum delay of 81.77ps, 150.1ns and 85.07ps respectively and average carry delay of 50.07ns. These adders consumes the average power of 152.8mW, 135.2mW and 145.8mW respectively. The Standard, D3L and sp-D3L adder in 90nm technology has a average sum delay of 33.82ps, 75.20ps and 16.74ns respectively and average carry delay of 50.02us, 50.07ns and 108.4ns respectively. These adders consumes the average power of 293.6mW, 261.6mW and 271.6mW respectively. And at last, The Standard, D3L and sp-D3L adder in 180nm technology has a average sum delay of 286ps, 284.6ps and 16.72ns respectively and average carry delay of 50.26ns, 50.64ns and 91.74ns respectively. These adders consumes the average power of 167.9mW, 136.8mW and 179.2mW respectively.

#### 4 CONCLUSION

The new split path Data Driven Dynamic Logic Implementation of the full adder is strong in terms of both performance-power-efficiency and drivability. This is very efficient when low power constraints are mandatory. Due to small, identically loaded gates the full adders designed using PROPOGATE and GENERATE functions, the full adder is observed to be the best in the performance.

The sp-D3L adders implemented here has the speed advantage however it consumes more power. The power consumption can be reduced, but the pre-charge propagation path delay affects the speed performance of the adder.

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